



PROJECT DESCRIPTION

Architecture design and programming for multicore-based Petaflop supercomputers

The Architecture design and programming for multicore-based Petaflop supercomputers project encompasses the efforts done at the Computer Architecture Department of the UPC (Technical University of Catalunya) and the Computer Sciences Department of the BSC-CNS (Barcelona Supercomputing Center) towards designing future petaflop supercomputing systems. The emerging era of multicore architectures, that will include hundreds of processors in a single chip, has pushed the research community to seek for new techniques to make it easier for application and library programmers to develop scalable and efficient multi-threaded applications. Heterogeneity in these multicores is also becoming a trend (for instance, the IBM Cell BE processor that mixes a traditional superscalar core and eight more specialized cores). GPGPU- and FPGA-based architectures will also play an important contribution to this heterogeneous world, leading to systems with millions of threads that cooperate in the efficient exploitation of parallelism for challenging scientific applications. The approximation taken by the UPC and BSC researchers considers the design of future petaflop systems in an interdisciplinary way, including applications, numerical methods, programming models, tools for performance analysis and prediction, node and interconnect design as well as processor/accelerator design.

RESPONSIBLE UPC RESEARCHER

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TYPE OF RESEARCH COOPERATION ENVISIONED

We primarily envision PhD students, although Post-Doc and sabbatical could also be interesting for the project.

FUNDING AND FACILITIES OFFERED

The Computer Architecture Department at UPC and the Computer Sciences Department at BSC offer grants for PhD students (equivalent to grants offered by national research programs) and the necessary equipment and access to supercomputing facilities to develop the research project.